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IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF	:
JEAN-LUC PERON	: EXAMINER: TORRES, J.A.
SERIAL NO: 10/806,524	:
FILED: MARCH 23, 2004	: GROUP ART UNIT: 2611
FOR: DATA PROCESSING APPARATUS AND METHOD OPERABLE TO MAP AND DE-MAP SYMBOLS AND CARRIER SIGNALS FO AN ORTHOGONAL FREQUENCY DIVISION MULTIPLEXED (OFDM) SYMBOL	:

COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

SIR:

Applicant acknowledges with appreciation the indication of allowability of the claimed invention. In response to the Examiner's Statement of Reason for Allowance in the Notice of Allowance of August 8, 2008, Applicant respectfully submits the following comments.

The Examiner's statement of reasons for allowance on pages 2-3 of the Notice of Allowance mailed August 8, 2008, states:

> Claims 1-15 are allowed because a comprehensive search of prior art failed to teach, either alone or in combination, an address generator for use with transmission or reception of data symbols interleaved onto substantially four thousand carriers of an Orthogonal Frequency Division Multiplexed symbol, the address generator being operable to generate a set of addresses, each address being generated for each of the data symbols to indicate one of the carrier signals onto which the data symbol is to be mapped or de-mapped, the address generator comprising a linear feedback shift register including a predetermined number

of register stages and being operable to generate a pseudo-random bit sequence in accordance with a generator polynomial, a permutation circuit operable to receive the content of the shift register stages and to permute the bits present in the registered stages in accordance with a permutation order to form an address of one of the OFDM carriers, and to a control unit operable in combination with an address check circuit to re-generate an address when a generated address exceeds the predetermined number of carriers, characterised in that the linear feedback shift register has eleven register stages with a generator polynomial for the linear feedback shift register of $R_i'[10]=R_{i-1}'[0] \oplus R_{i-1}'[2]$, and the permutation order forms an eleven bit address $R_i[n]$ for the i-th data symbol from the bit present in the n-the register stage $R_i'[n]$ in accordance with the table:

$R_i'[n]$ for n =	10	9	8	7	6	5	4	3	2	1	0
$R_i[n]$ for n =	7	10	5	8	1	2	4	9	0	3	6

However, it is respectfully noted that the features recited in Applicants' Claim 1 differ from the elements recited above. For example, Claim 1 does not recite "an address generator for use with transmission or reception of data symbols interleaved onto substantially four thousand carriers of an Orthogonal Frequency Division Multiplex symbol." Further, it is respectfully submitted that the above-quoted statement also does not apply to independent Claims 6, 9, and 11-15 (and all claims depending thereon) either, as these claims have different claim scope than Claim 1 (e.g. independent Claims 11 and 12 are method claims and independent Claims 14 and 15 recite means-plus-function language.)

Respectfully submitted,

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